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(57) **ABSTRACT**

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A light emitting display for improving image quality and a Thin Film Transistor (TFT) includes at least one data line for transmitting a data signal, at least one scanning line for transmitting a selected signal, and at least one pixel electrically connected to the data line and the scanning line. The pixel includes a first TFT for responding to the selected signal and transmitting the data signal to an organic light emitting device, a capacitor electrically connected to the first TFT and storing a voltage corresponding to the transmitted data signal, a second TFT connected to the capacitor and supplying an organic light emitting device with a current corresponding to the data signal selected by the selected signal. The widths of respective channel regions of the first TFT are different from each other to reduce the kickoff voltage and improve the driving ability of the TFT, thereby improving the image quality of the light emitting display.

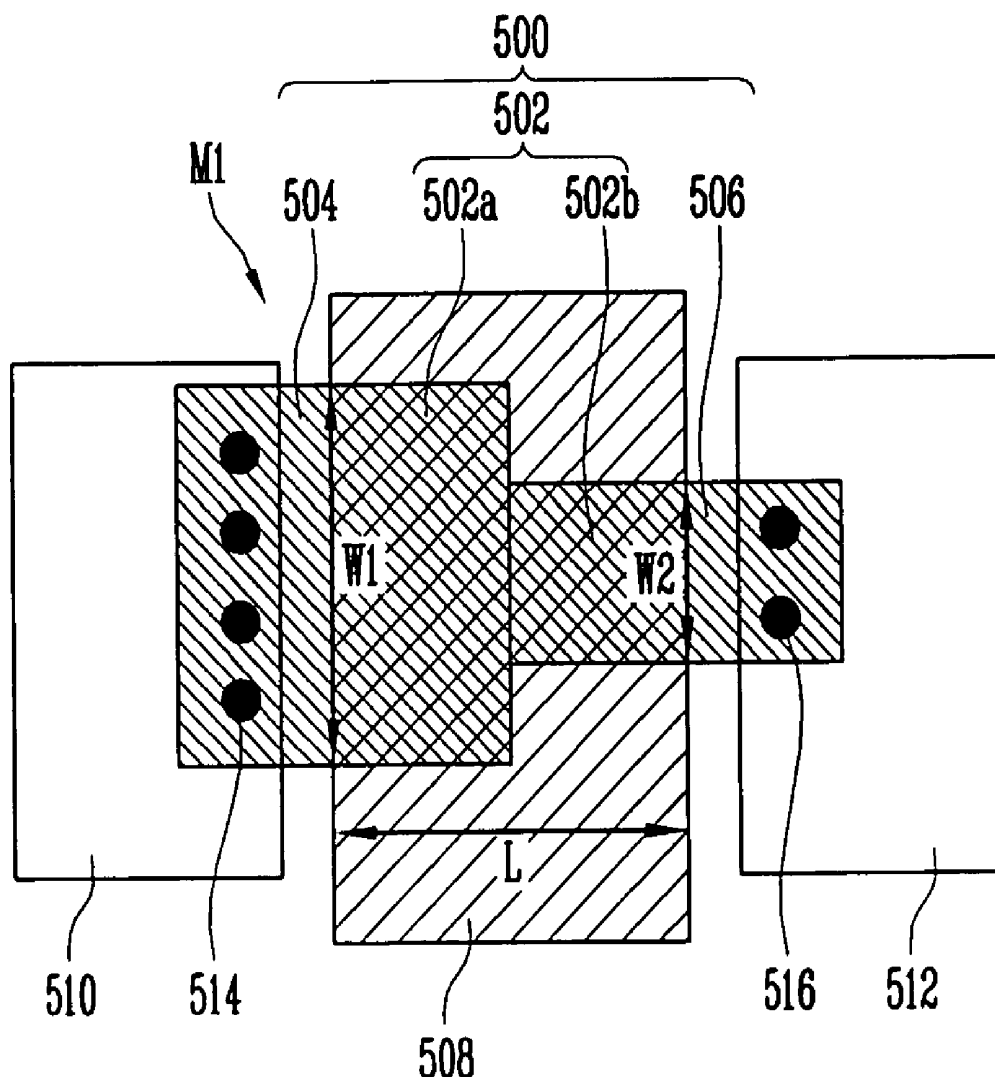


FIG. 1

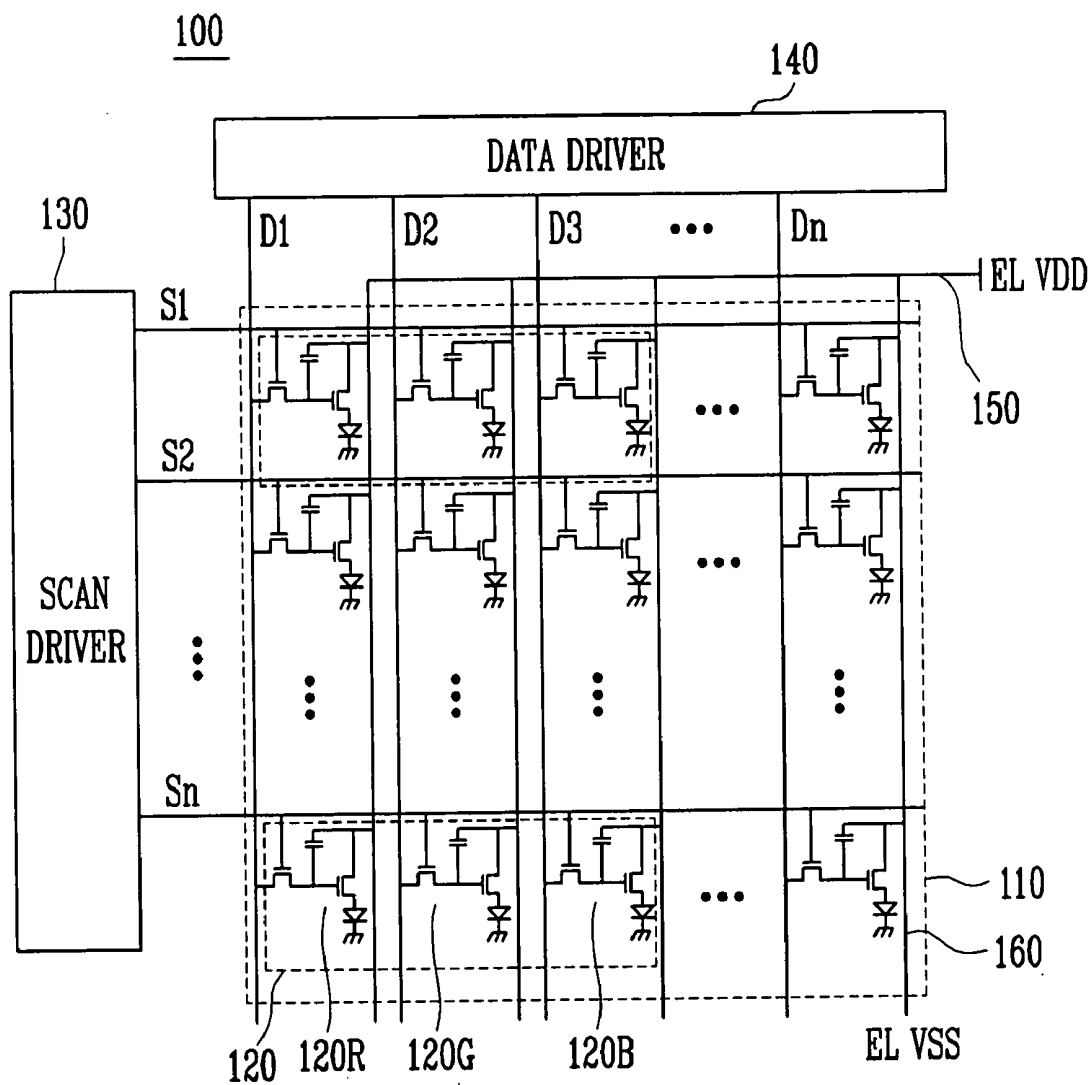


FIG. 2

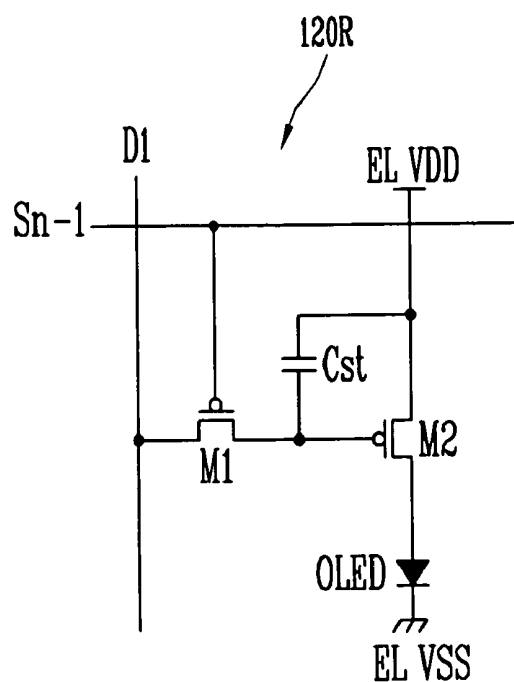


FIG. 3

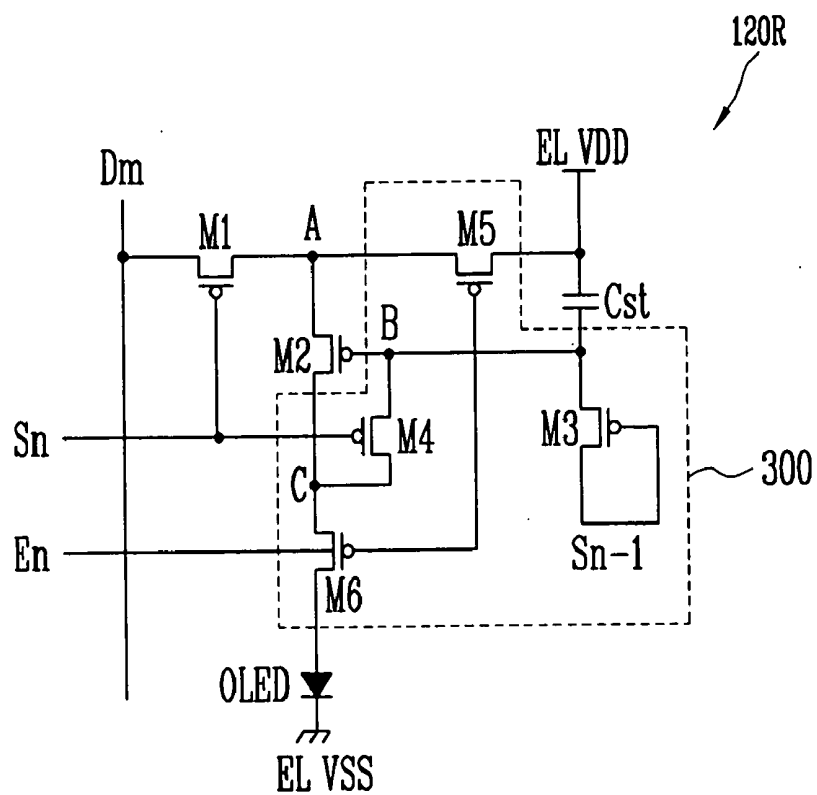


FIG. 4

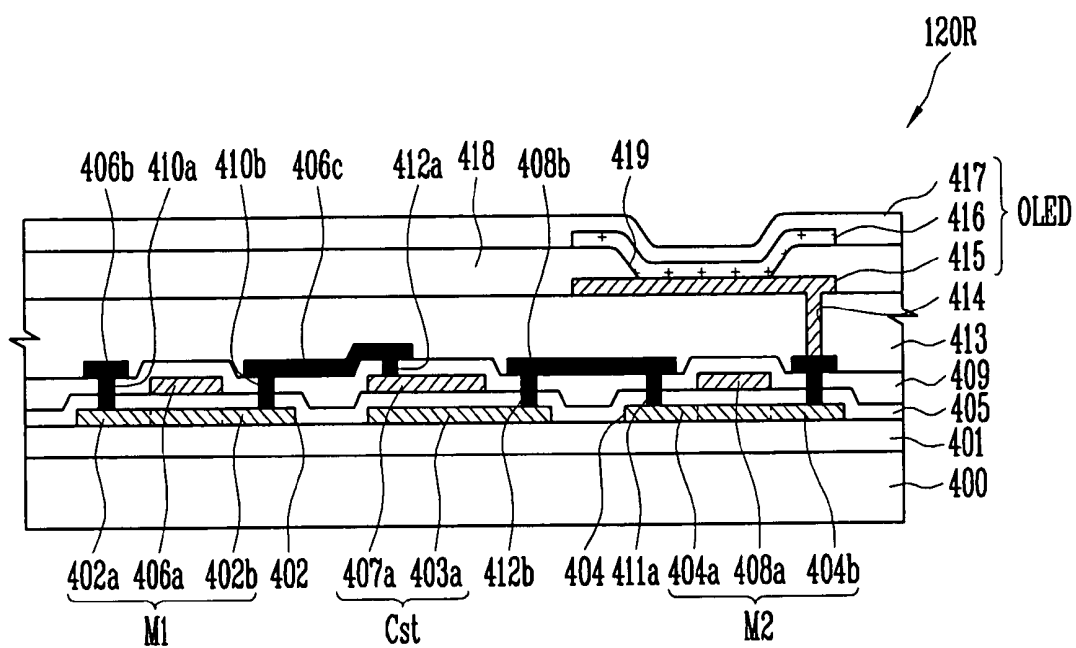
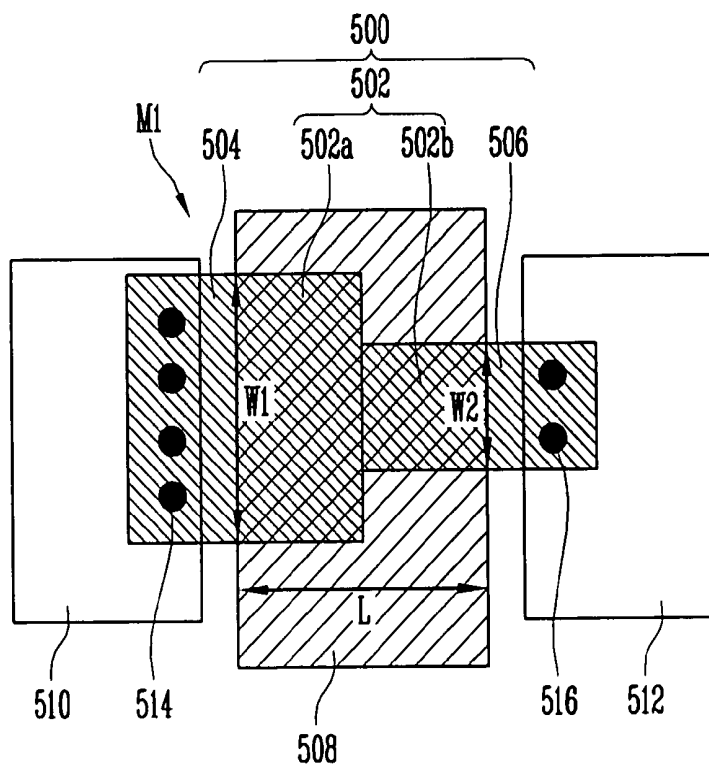


FIG. 5



LIGHT EMITTING DISPLAY AND THIN FILM TRANSISTOR (TFT)

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from an application for LIGHT EMISSION DISPLAY AND THIN FILM TRANSISTOR earlier filed in the Korean Intellectual Property Office on 22 Jun. 2005 and there duly assigned Serial No. 10-2005-53975.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a light emitting display and a Thin Film Transistor (TFT), and more particularly, to a TFT having improved driving ability by reducing off-current and a light emitting display having enhanced image quality using the TFT.

[0004] 2. Description of the Related Art

[0005] Generally, an active matrix type light emitting display includes at least a single data line for transmitting a data signal, at least a single scanning line for transmitting a selecting signal, and a plurality of image pixels electrically connected to the data line and the scanning line. Generally, each image pixel includes a light emitting device, a capacitor for storing voltage corresponding to the data signal transmitted from the data line, and at least two Thin Film Transistors (TFTs) for controlling the light emitting device. As described above, the structure of the image pixel including two TFTs and a single capacitor is '2TR+1Cap' structure.

[0006] In the 2TR+1Cap structure, one of the two TFTs serves to as a switching device for responding the selecting signal and transmitting the data signal to the light emitting device, and the other serves to as a driving device for supplying electric current to corresponding to the selected data signal to the light emitting device. The TFTs are manufactured to have a semiconductor layer, a gate insulating layer, a gate electrode, and source/drain electrodes laminated in turn, and are generally divided into a staggered type TFT and a coplanar type TFT. Moreover, according to the formation position of the gate electrode with respect to the source/drain electrodes, the TFTs are divided into an upper gate structured TFT and a lower gate structured TFT.

[0007] For example, the upper gate structured TFT includes a semiconductor layer formed on a substrate, a gate insulating layer formed on the semiconductor layer, a gate electrode formed on the gate insulating layer, and source/drain electrodes. The semiconductor layer includes source and drain regions doped with impurities of a predetermined concentration, and a channel region formed between the source and drain regions. The gate electrode is generally formed on the gate insulating layer on the channel region, and the source/drain electrodes are respectively connected to the source and drain regions through contact holes while interposing interlayer-insulating layer on the gate electrode.

[0008] In the light emitting display including the image pixels having the two TFTs and the capacitor, when leakage current of the switching TFT turning on/off a driving TFT is large, the capacitor cannot maintain data voltage uniform.

Thus, in the light emitting display, crosstalk, flicker, and so on are caused, and further image quality of the light emitting display may be deteriorated.

[0009] In order to overcome the above-mentioned problems and improve the image quality of the light emitting display including the image pixels having the 2TR+1Cap structure, addition of complementing circuits to the image pixels is proposed.

[0010] However, since, when the complementation circuits are added to the image pixel structure, a plurality of TFTs must be added, driving method thereof becomes relatively complex in comparison to the conventional image pixel structure. Moreover, since, in the image pixel structure including the complementation circuit, there is a high possibility of leakage current through the path from the capacitor to the plural TFTs, the ability of the capacitor for maintaining voltage is relatively deteriorated. In other words, although the complementation circuit is added to the image pixel structure, the image quality of the light emitting display may be deteriorated.

[0011] Additionally, terminals of every device constituting the image pixel are affected by kickback voltage generated by the peak-to-peak of a gate signal used in a single image pixel, that is, the voltage difference raging from EL VDD to EL VSS. Moreover, when the kickback voltage, generated by a terminal to which the capacitor is connected, is increased, voltage for driving the light emitting devices is affected so that the image quality is deteriorated.

SUMMARY OF THE INVENTION

[0012] Therefore, the present invention has been made to overcome the above-mentioned problems, and it is an object of the present invention to provide a Thin Film Transistor (TFT) in which widths of end sides of channel regions of switching TFTs constituting an image pixel are different from each other so that off-current is decreased and driving ability is improved, and a light emitting display having improved image quality.

[0013] In accordance with the present invention, the above and other objects can be accomplished by the provision of a light emitting display including: at least one data line adapted to transmit a data signal; at least one scanning line adapted to transmit a selected signal; at least one pixel electrically connected to the data line and the scanning line, the pixel including: a first TFT adapted to respond to the selected signal and to transmit the data signal to an organic light emitting device, and a capacitor electrically connected to the first TFT and adapted to store a voltage corresponding to the transmitted data signal; and a second TFT connected to the capacitor and adapted to supply the organic light emitting device with a current corresponding to the data signal selected by the selected signal; respective widths of channel regions of the first TFT are different from each other.

[0014] One end of a channel region having a smallest width among the widths of the channel regions of the first TFT is preferably electrically connected to one electrode of the capacitor.

[0015] One end of a channel region having a smallest width among the widths of ends of the channel regions of the first TFT is preferably electrically connected to a gate electrode of the second TFT.

[0016] One end of a channel region having a smallest width among the widths of ends of the channel regions of the first TFT preferably includes a drain electrode of the first TFT.

[0017] The first TFT preferably includes a dual gate structure. The first TFT preferably includes a dual gate structure.

[0018] The pixel preferably further includes a threshold voltage compensation circuit adapted to compensate a threshold voltage of the second TFT. The pixel preferably further includes a voltage drop compensation circuit adapted to compensate a voltage drop of a first voltage supplied to the pixel.

[0019] The first TFT preferably includes a structure selected from a group of structures including a coplanar structure, a staggered structure, an upper gate structure, and a lower gate structure.

[0020] In accordance with the present invention, the above and other objects can be accomplished by the provision of a TFT including: a semiconductor layer including a channel region having a width of one end thereof greater than a width of another end thereof and having source and drain regions arranged in the ends of the channel region; source and drain electrodes electrically connected to the semiconductor layer; an insulating layer contacting the channel region; and a gate electrode facing the channel region and having the insulating layer interposed therebetween.

[0021] The another end of the channel region is preferably electrically connected to the drain region.

[0022] The TFT preferably further includes a dual gate structure, the channel region and the gate electrode respectively preferably including first and second channel regions and first and second gate electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] A more complete appreciation of the present invention, and many of the attendant advantages thereof, will be readily apparent as the present invention becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

[0024] **FIG. 1** is a circuit diagram of a light emitting display according to an embodiment of the present invention;

[0025] **FIG. 2** is a partially enlarged view of the light emitting display of **FIG. 1**;

[0026] **FIG. 3** is a circuit diagram of a light emitting display according to another embodiment of the present invention;

[0027] **FIG. 4** is a schematic side sectional view of the light emitting display of **FIG. 2**;

[0028] **FIG. 5** is a plan view of a Thin Film Transistor (TFT) according to a first embodiment of the present invention; and

[0029] **FIG. 6** is a plan view of a TFT according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0030] Hereinafter, exemplary embodiments according to the present invention are described below with reference to the accompanying drawings.

[0031] **FIG. 1** is a circuit diagram of a light emitting display according to an embodiment of the present invention, and **FIG. 2** is a partially enlarged view of the light emitting display of **FIG. 1**.

[0032] As shown in **FIG. 1**, a light emitting display 100 includes an image display 110 having a plurality of image pixels 120, a scan driver 130 for transmitting a selected signal to the image display 110 through a plurality of scanning lines S1, S2, to Sn, and a data driver 140 for transmitting a data signal to the image display 110 through a plurality of data lines D1, D2, D3, to Dm.

[0033] The image display 110 includes a plurality of image pixels having sub-image pixels 120R, 120G, and 120B for displaying Red (R), Green (G), and Blue (B). Each of the image pixels 120 is connected to the scanning lines S1 to Sn to which the selected signal such as the scanning signal are transmitted, the data lines D1 to Dm for transmitting the data signal, a first power line 150 for supplying a first voltage EL VDD, and a second power line 160 for supplying a second voltage EL VSS.

[0034] As shown in **FIG. 2**, the sub-image pixel 120R of the image pixel 120 includes an organic light emitting device (OLED), a first Thin Film Transistor (TFT) M1, a capacitor Cst, and a second TFT M2. Moreover, a scanning line Sn-1 connected to one of the first TFT M1, the capacitor Cst, and the second TFT M2, the data line D1, and the first power line EL VDD are connected to the sub-image pixel 120R. The scanning line Sn-1 is formed in the row direction, and the data line D1 and the power line EL VDD are formed in the column direction. The first TFT M1 serves as a switching device for responding to the selected signal and transmitting the data signal to the OLED, and the second TFT M2 serves as a driving device for supplying an electrical current corresponding to the data signal selected by the selected signal to the OLED.

[0035] The above-mentioned sub-image pixel 120R displays an image according to the following driving principle. When the scanning signal is supplied to a gate electrode of the first TFT M1, the first TFT M1 is turned on. When the first TFT M1 is turned on, the capacitor Cst is charged by a voltage corresponding to the data signal and the voltage of the capacitor Cst is supplied to the gate electrode of the second TFT M2. By doing so, the second TFT M2 supplies an electrical current to OLED such that every OLED contained in each of sub-image pixel 120a is lit.

[0036] **FIG. 3** is a circuit diagram of a light emitting display according to another embodiment of the present invention. As shown in **FIG. 3**, the electric circuit in **FIG. 3** includes a threshold voltage compensating circuit for compensating the threshold voltage to the 2TR+1Cap structure of the circuit of **FIG. 2**.

[0037] The sub-image pixel 120R of **FIG. 3** includes an organic light emitting device OLED, the first TFT M1 serving as a switching device, the second TFT M2 serving as a driving device, the capacitor Cst, and the threshold

compensating circuit 300. The threshold compensating circuit 300 includes a third TFT M3, a fourth TFT M4, a fifth TFT M5, and a sixth TFT M6.

[0038] The first to sixth TFTs M1, M2, M3, M4, M5, and M6 respectively include gate electrodes, source electrodes, and drain electrodes, and the capacitor Cst includes a first electrode and a second electrode.

[0039] The gate electrode of the first TFT M1 is connected to nth scanning line Sn, the source electrode of the first TFT M1 is connected to the data line Dm, and the drain electrode of the first TFT M1 is connected to a first node A. The data signal is transmitted to the first node A in response to an nth scanning signal inputted through the scanning line Sn.

[0040] The source electrode of the second TFT M2 is connected to the first node A, the drain electrode of the second TFT M2 is connected to a third node C, and a gate electrode of the second TFT M2 is connected to a second node B. When the electrical potential of the second node B is equal to the electrical potential of the third node C by the fourth TFT M4, the second TFT M2 serves as a diode, so that the data signal transmitted to the first node A reaches the second node B via the second TFT M2. When electrical power for the image pixel is supplied to the first node A through the image power line EL VDD, an electrical current corresponding to the voltage supplied to the gate electrode flows from the source electrode to the drain electrode. In other words, a current flow due to the electrical potential of the second node B is determined.

[0041] A gate electrode of the third TFT M3 is connected to the n-lth scanning line Sn-1 and a drain electrode of the third TFT M3 is connected to the second node B. The nth scanning signal inputted through the n-lth scanning line Sn-1 is transmitted to the second node B.

[0042] A gate electrode of the fourth TFT M4 is connected to the nth scanning line Sn, a source electrode of the fourth TFT M4 is connected to the third node C, and a drain electrode of the fourth TFT M4 is connected to the second node B. The electrical potential of the second node B is identical to the electric potential of the third node C in response to the nth scanning signal inputted through the nth scanning line Sn.

[0043] A source electrode of the fifth TFT M5 is connected to the image pixel power line EL VDD, a drain electrode of the fifth TFT M5 is connected to the first node A, and a gate electrode of the fifth TFT M5 is connected to a light emitting controlling line En. The image pixel electrical power is selectively transmitted to the second TFT M2 in response to a light emitting controlling signal transmitted through the light emitting controlling line En.

[0044] A source electrode of the sixth TFT M6 is connected to the third node C, a drain electrode of the sixth TFT M6 is connected to the organic light emitting device OLED, and a gate electrode of the sixth TFT M6 is connected to the light emitting controlling line En. Electrical current is selectively transmitted to the organic light emitting device OLED in response to the light emitting controlling signal transmitted through the light emitting controlling line En.

[0045] A first electrode of the capacitor Cst is connected to the image pixel power line EL VDD and a second electrode of the capacitor Cst is connected to the second node B. When

an initial signal is supplied to the second node B by the third TFT M3, the initial signal is transmitted to the capacitor Cst, and the capacitor Cst receiving the initial signal stores the initial voltage and charges to a voltage corresponding to the data signal when the data signal is transmitted to the second TFT M2 by the first TFT M1 and the fourth TFT M4. The capacitor Cst transmits the stored voltage to the second node B such that the voltage stored in the capacitor Cst is supplied to the gate electrode of the second TFT M2.

[0046] Hereinafter, elements of the sub-image pixel 120R are described in detail below with reference to FIG. 4, a schematic side sectional view of the circuit of the light emitting display of FIG. 2.

[0047] As shown in FIG. 4, the sectional structure of the sub-image pixel 120R includes a buffer layer 401 formed on an insulating substrate 400 such as glass in a form of a nitride film or an oxide film. The buffer layer 401 prevents impurities such as metal ions from spreading into an active channel in the semiconductor layer.

[0048] An amorphous silicon layer is then formed by a process, such as Chemical Vapor Deposition (CVD), sputtering, or the like, on the substrate 400 formed with the buffer layer 401. The amorphous silicon layer is formed of semiconductor layers 402 and 404 by solid phase crystallization, such as SPC, MIC, SGS, or the like, and liquid phase recrystallization, such as ELA. Simultaneously, a lower electrode 403a of the capacitor Cst is formed. The semiconductor layers 402 and 404 can be formed such that the amorphous silicon layer is laminated on the substrate and crystallized into a polysilicon layer, or the polysilicon layer is directly laminated on the buffer layer 401 and is processed by patterning.

[0049] The semiconductor layers 402 and 404 can be patterned in a predetermined shape in order to provide transfer characteristics different from that of the second TFT M2 serving as a driving device to the first TFT M1 serving as a switching device in the present invention. The light emitting ability of the organic light emitting device OLED exhibits a brightness difference according to the current supplied to the organic light emitting device OLED. In other words, an organic light emitting device with excellent light emitting ability can exhibit a brightness higher than those of other organic light emitting devices when equal currents are supplied thereto. The detailed shape of the patterned semiconductor layer 402, for improving the light emitting efficiency of the organic light emitting device OLED, is described later with reference to FIGS. 5 and 6.

[0050] A gate insulating layer 405 is formed on the semiconductor layers 402 and 404, and gate electrodes 406a and 408a are formed on the gate insulating layer 405. An upper electrode 407a of the capacitor Cst is formed together with the gate electrodes 406a and 408a. Next, impurities are doped using the gate electrodes 406a and 408a as masks to form source and drain regions 402a, 402b, 404a, and 404b. The semiconductor layers 402 and 404 located at the lower side of the gate electrodes 406a and 408a become the channel regions, and doping regions formed in the lateral sides of the channel regions become respectively the source regions 402a and 404a and the drain regions 402b and 404b.

[0051] An interlayer insulating film 404 is formed on the upper side of the above-mentioned structure, and first and

second contact holes **410a**, **411a**, **410b** and **411b** are formed on the interlayer insulating film **404**. The first and second contact holes **410a**, **411a**, **410b**, and **411b** respectively expose the source regions **402a** and **404a** and the drain regions **402b** and **404b** of the first TFT M1 and the second TFT M2. Third contact holes **412a** and **412b** for exposing the upper electrode **407a** of the capacitor Cst can be formed together with the first and second contact holes **410a**, **411a**, **410b**, and **411b**. Source electrodes **406b** and **408b** and drain electrodes **406c** and **408c**, respectively connected to the source regions **402a** and **404a** and the drain regions **404a** and **404b** via the first and second contact holes **410a**, **411a**, **410b**, and **411b**, are formed on the interlayer insulating layer.

[0052] A protection layer **413** is formed on the source and drain electrodes **406b**, **408b**, **406c**, and **408c**. A fourth contact hole **414** for exposing the drain electrode **408c** of the second TFT M2 is formed in the protection layer **413**. A first electrode **415** (hereinafter referred to as an anode electrode) of the organic light emitting device OLED is formed on the protection layer **413**. The anode electrode **415** is electrically connected to the drain electrode **408c** of the second TFT M2 via the fourth contact hole **414**. A pixel definition layer **418** is formed on the anode electrode **415**, and an opening **419** for exposing the anode electrode **415** is formed in the pixel definition layer **418**. A light emitting layer **416** is formed in the opening **419**. A second electrode **417** (cathode electrode) of the organic light emitting device OLED is formed on the light emitting layer **416**.

[0053] Through the above-mentioned laminating order, the first TFT M1, including the source electrode **406b** connected to the source region **402a** of the semiconductor layer **402**, the drain electrode **406c** connected to the drain region **402b**, and the gate electrode **406a** formed on the semiconductor layer **402**, is formed. Moreover, the second TFT M2, including the source electrode **408b** connected to the source region **404a** of the semiconductor layer **404**, the drain electrode **408c** connected to the drain region **404b**, and the gate electrode **408a** formed on the semiconductor layer **404**, is formed. The capacitor Cst comprises the lower electrode **403a** and the upper electrode **407a**. The organic light emitting device OLED comprises the anode electrode **415**, the light emitting layer **416**, and the cathode electrode **417**.

[0054] In this embodiment, although the method of manufacturing image pixels including PMOS-structured TFTs has been described, the present invention is not limited to this and can be easily applied to methods of manufacturing image pixels including other TFTs such as NMOS- or CMOS-structured TFTs. Although, with respect to FIG. 4, the sectional structure of the image pixels including the upper gate type or coplanar type first TFT M1 served to as a switching device has been described, such sectional structure can be applied almost like the sectional structures of the other sub-image pixels **120G** and **120B**. Moreover, although this embodiment of the present invention discloses the side sectional view of the light emitting display in FIG. 2 illustrating the circuit diagram of the 2TR+1Cap structure, a side sectional view of the light emitting display can be described with reference to FIG. 4 including a threshold voltage compensation circuit.

[0055] Hereinafter, the pattern of the first TFT M1 serving as a switching device is described in detail with reference to

FIGS. 5 and 6, which are plan views illustrating the TFT of the light emitting display according to an embodiment of the present invention.

[0056] As shown in FIG. 5, the channel region of the first TFT M1 has a first width W1 and a second width W2, and the length L of the channel region has a first channel length L1 and a second channel length L2 and represents an effective channel length. An end having a smaller width W2 of the widths W1 and W2 of the channel region of the first TFT M1 is electrically connected to one of electrodes of the capacitor Cst and the gate electrode of the second TFT M2, and the end having the smaller width W2 of the channel region is the drain electrode of the first TFT M1.

[0057] In detail, the first TFT M1 includes a semiconductor layer **500**, a gate electrode **508**, a drain electrode **510**, and a source electrode **512**. The semiconductor layer **500** includes channel regions **502** (**502a** and **502b**) formed in the lower side of the gate electrode **508**, and drain region **504** and source region **506**, formed at the lateral sides of the channel regions **502**. The drain electrode **510** is electrically connected to the drain region **504** via at least a single first contact hole **514**, and the source electrode **512** is electrically connected to the source region **506** via at least a single second contact hole **516**.

[0058] As shown in FIG. 6, the channel region of the first TFT M1 has a first width W1 and a second width W2, and two effective channel lengths L1 and L2. In this embodiment of the present invention, the first TFT M1 has a dual gate structure. In the dual gate structured first TFT M1, an end having a smaller width W2 of the widths W1 and W2 of the channel region is electrically connected to one of electrodes of the capacitor Cst and the gate electrode of the second TFT M2, and the other end having the second width W2 is the drain electrode of the first TFT M1.

[0059] In detail, the first TFT M1 in FIG. 6 includes a semiconductor layer **600**, a gate electrode **608**, a drain electrode **610**, and a source electrode **612**. The semiconductor layer **600** includes channel regions **602** (**602a** and **602b**) formed in the lower side of the gate electrode **608**, and a drain region **604** and a source region **606** formed in the lateral sides of the channel regions **602**. The drain electrode **610** is electrically connected to the drain region **604** via at least a single first contact hole **614**, and the source electrode **612** is electrically connected to the source region **606** via at least a single second contact hole **616**.

[0060] As shown in FIGS. 5 and 6, respective the widths W1 and W2 of the channel regions **502** and **602** of the first TFT M1 have multiple steps. As such, the widths of the ends of the channel regions **502** and **602** of the first TFT M1 are different from each other so that off-current can be reduced and kickback voltage can be also reduced. Generally, since the kickback voltage is affected by the overlapped area between the channel regions **502** and **602** and the gate electrodes **508** and **608** with respect to the central region of the channel regions **502** and **602**, the kickback voltage can be reduced by decreasing the width of a channel region contacting a terminal causing the kickback phenomenon.

[0061] Particularly, the kickback voltage can be reduced by decreasing the width of the channel region connected to the gate of the second TFT M2 serving as a driving device. When the TFT serving as a switching device is so structured,

the kickback voltage and the off-current can be reduced even in the pixel structure including the compensation circuit in which a relatively high leakage current is generated by a plurality of TFT paths.

[0062] Although the above-described embodiment is applied to the pixel structure (2TR+1Cap) including two TFTs and a single capacitor and a pixel structure further including the threshold voltage compensation circuit for compensating threshold voltage of the second TFT having the 2TR+1Cap structure, the present invention is not limited to these, but can be applied to a pixel structure further including a voltage drop compensation circuit for compensating for the voltage drop of a first electrical power and other various pixel image structures. Moreover, although, in the above-mentioned embodiment, the length of the first channel region of the channel regions is equal to the length of the second channel region, the length of the first channel region can be different from the length of the second channel region.

[0063] As described above, according to the present invention, the widths of ends of the channel regions of the TFT are different from each other so that the kickback voltage and the off-current of the TFT can be reduced. Therefore, the image quality of the light emitting display adopting the above-mentioned TFT can be improved.

[0064] Although exemplary embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that modifications can be made to these embodiments without departing from the principles and spirit of the present invention, the scope of which is defined by the following claims.

What is claimed is:

1. A light emitting display, comprising:

at least one data line adapted to transmit a data signal;

at least one scanning line adapted to transmit a selected signal;

at least one pixel electrically connected to the data line and the scanning line, the pixel including: a first Thin Film Transistor (TFT) adapted to respond to the selected signal and to transmit the data signal to an organic light emitting device, and a capacitor electrically connected to the first TFT and adapted to store a voltage corresponding to the transmitted data signal; and

a second Thin Film Transistor (TFT) connected to the capacitor and adapted to supply the organic light emitting device with a current corresponding to the data signal selected by the selected signal;

wherein respective widths of channel regions of the first TFT are different from each other.

2. The light emitting display according to claim 1, wherein one end of a channel region having a smallest width among the widths of the channel regions of the first TFT is electrically connected to one electrode of the capacitor.

3. The light emitting display according to claim 1, wherein one end of a channel region having a smallest width among the widths of ends of the channel regions of the first TFT is electrically connected to a gate electrode of the second TFT.

4. The light emitting display according to claim 2, wherein one end of a channel region having a smallest width among the widths of ends of the channel regions of the first TFT comprises a drain electrode of the first TFT.

5. The light emitting display according to claim 3, wherein one end of a channel region having a smallest width among the widths of ends of the channel regions of the first TFT comprises a drain electrode of the first TFT.

6. The light emitting display according to claim 4, wherein the first TFT comprises a dual gate structure.

7. The light emitting display according to claim 5, wherein the first TFT comprises a dual gate structure.

8. The light emitting display according to claim 1, wherein the pixel further comprises a threshold voltage compensation circuit adapted to compensate a threshold voltage of the second TFT.

9. The light emitting display according to claim 1, wherein the pixel further comprises a voltage drop compensation circuit adapted to compensate a voltage drop of a first voltage supplied to the pixel.

10. The light emitting display according to claim 1, wherein the first TFT comprises a structure selected from a group of structures including a coplanar structure, a staggered structure, an upper gate structure, and a lower gate structure.

11. A Thin Film Transistor (TFT), comprising:

a semiconductor layer including a channel region having a width of one end thereof greater than a width of another end thereof and having source and drain regions arranged in the ends of the channel region;

source and drain electrodes electrically connected to the semiconductor layer;

an insulating layer contacting the channel region; and

a gate electrode facing the channel region and having the insulating layer interposed therebetween.

12. The TFT as claimed in claim 11, wherein the another end of the channel region is electrically connected to the drain region.

13. The TFT as claimed in claim 11, further comprising a dual gate structure, wherein the channel region and the gate electrode respectively include first and second channel regions and first and second gate electrodes.

* * * * *

专利名称(译)	发光显示器和薄膜晶体管 (TFT)		
公开(公告)号	US20060290633A1	公开(公告)日	2006-12-28
申请号	US11/448684	申请日	2006-06-08
[标]申请(专利权)人(译)	CHOI WOONG SIK		
申请(专利权)人(译)	CHOI , WOONG植		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	CHOI WOONG SIK		
发明人	CHOI, WOONG-SIK		
IPC分类号	G09G3/36		
CPC分类号	H01L27/12 H01L27/1214 H01L29/78696 H01L29/78645 H01L27/3244 H01L27/124		
优先权	1020050053975 2005-06-22 KR		
其他公开文献	US9196747		
外部链接	Espacenet USPTO		

摘要(译)

用于改善图像质量的发光显示器和薄膜晶体管 (TFT) 包括用于传输数据信号的至少一条数据线, 用于传输所选信号的至少一条扫描线, 以及电连接到数据线的至少一个像素和扫描线。该像素包括: 第一TFT, 用于响应所选择的信号并将数据信号传输到有机发光器件; 电容器, 电连接到第一TFT并存储对应于传输的数据信号的电压; 第二TFT, 连接到电容器向有机发光器件提供与由所选信号选择的数据信号相对应的电流。第一TFT的各个沟道区的宽度彼此不同, 以降低启动电压并改善TFT的驱动能力, 从而提高发光显示器的图像质量。

